Amendments to the Specification:

Please replace the first paragraph under the Description of the Prior art which begins on page 1, line 22 with the following amended paragraph:

Data processing systems are systems that manipulate, process, and store data, and are well known in the art. Personal computer systems and their associated circuitry are such data processing systems. Fig.1 is a diagram of a prior art computer system 10. The computer system 10 comprises a central processing unit (CPU) 12, a north bridge circuit 14, a south bridge circuit 16, a display controller 18, a memory device 20, an I/O device 22, and a hard-disk drive 24. The CPU 12 is used to control the operation of the computer system 10. The north bridge circuit 14 is used to arbitrate signals transmitted between the CPU 12 and high-speed peripheral devices such as the display controller 18 and the memory device 20. The display controller 18 is used to handle display data, and the memory device 20 is used to process and store data. The south bridge circuit 16 is used to arbitrate signals transmitted between the north bridge circuit 14 and low-speed peripheral devices such as the I/O device 22 and the hard-disk drive 24. The I/O device 22 (a keyboard for example) is used to receive control signals inputted by an end-user. The hard-disk drive 24 usually is a non-volatile memory device, while the memory device 20 usually is a volatile memory device. The memory device 20 may include a dynamic random access memory (DRAM) to store processing programs and data. For example, the programs and data stored on the hard-disk drive 24 are loaded into the memory device 20 so that the CPU 12 is capable of executing the programs more quickly. Then, the data processed by the CPU 12 are stored back to the memory device 20. It is noted that the north bridge circuit 14 has a memory controller 26 for controlling the access of the memory device 20. When a master device such as the CPU 12 or the display controller 18 issues access requests to the memory controller 26, the memory controller 26 accesses the memory device 20 according to the received access requests. With an in-order access scheme, the memory controller 26 responds to the master device according to the order of the received

access requests. For example, the display controller 18 outputs read requests RA1, RA2, RA3, RA4, and RA5 in an order to acquire data D1, D2, D3, D4, and D5 stored in the memory device 20 respectively. Even the memory controller 26 executes the read requests RA1, RA2, RA3, RA4, and RA5 out of its original order, the memory controller 26 will still orderly transmit the retrieved data D1, D2, D3, D4, and D5 to the display controller 18.

Please replace the first paragraph on page 14 with the following amended paragraph:

The read requests RB1, RB2 now both retrieve data stored on the same page B. However, the read request RB1 is the last one in the request queue 40. The read request ~~RA2~~ RB2, therefore, is just pushed into the request queue 40 (steps 106, 104) and is stored in the queue entry Q4. In addition, the initial value is assigned to the monitoring register M4 corresponding to the queue entry Q4. The reordering parameters now have become: